REMARKS/ARGUMENTS

The Applicants originally submitted Claims 1-21 in the application. The Examiner has indicated that original Claims 15-21 are allowed. In the present response, the Applicants have amended Claims 1 and 8. No claims have been added or canceled. Accordingly, Claims 1-21 are currently pending in the application.

I. Rejection of Claims 1-5 and 8-12 under 35 U.S.C. §102

The Examiner has rejected Claims 1-5 and 8-12 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,160,213 to Arnold, *et al.* (Arnold). The Applicants respectfully disagree.

Arnold is directed to electronic musical instruments having a computer-based control system. (Column 1, lines 13-15). Arnold discloses a music information management system (MIMS) that includes a main processor CPU and a MIDI co-processor. (Column 5, lines 14-19 and Figure 2). The main processor CPU and the MIDI co-processor have access to each other's memory. (Column 12, lines 19-22). Due to a difference in bus architecture in a preferred embodiment, a conversion must occur for proper communication between the main processor CPU and the MIDI co-processor. (Column 12, lines 59-63). Additionally, the MIDI co-processor has separate instructions for addressing memory and I/O devices. To adjust, a separate space is assigned in the MIDI co-processor address space to generate the appropriate I/O access timing and signals in the main processor address space so that when the MIDI co-processor accesses the address space that is reserved for main processor memory space, the appropriate memory access timing and signals are generated. (Column 13, lines 17-27).

Arnold does not teach, however, a multi-protocol bus system employing a plurality of protocol indicators associated with an address space, each of the plurality of protocol indicators associated with a segment of the address space and indicate a particular bus protocol of an external device as recited in independent Claims 1 and 8. On the contrary, Arnold teaches assigning a separate address space in the MIDI co-processor to generate appropriate signals for the MIDI co-processor to access a portion of its own address space. Thus, instead of a particular bus protocol of an external device associated with an address space, Arnold teaches a co-processor providing an adjusting for itself in an address space to compensate for accessing memory and I/O devices using separate instructions. (Column 13, lines 16-33).

Therefore, Arnold does not disclose each and every element of independent Claims 1 and 8 and Claims dependent thereon. Accordingly, Arnold does not anticipate Claims 1-5 and 8-12 and the Applicants respectfully request the Examiner to withdraw the §102 rejection and allow issuance thereof.

II. Rejection of Claims 6 and 13 under 35 U.S.C. §103

The Examiner has rejected Claims 6 and 13 under 35 U.S.C. §103(a) as being unpatentable over Arnold in view of U.S. Patent No. 5,715,419 to Szczepanek, *et al.* (Szczpanek). As discussed above Arnold does not teach a multi-protocol bus system employing a plurality of protocol indicators associated with an address space, each of the plurality of protocol indicators associated with a segment of the address space and indicate a particular bus protocol of an external device as recited in independent Claims 1 and 8. Instead, Arnold teaches a co-processor that accesses memory and I/O devices differently and adjusts accordingly to provide proper access to the co-processor memory.

(Column 13, lines 16-28). Thus, Arnold does not teach or suggest each and every element of independent Claims 1 and 8.

Szczepanek is directed to an improved data communications system and method for operating. (Column 1, lines 5-8). Szczepanek has not been cited to cure the deficiencies of Arnold but to teach dividing an address space into 4 kilobyte address ranges. (Examiner's Action, page 3). Thus, the cited combination of Arnold and Szczepanek does not teach or suggest each and every element of independent Claims 1 and 8.

Since the cited combination of Arnold and Szczepanek fails to teach or suggest each and every element of independent Claims 1 and 8 Claims dependent thereon, Claims 6 and 13 are not obvious in view of the cited combination. Accordingly, the Applicants respectfully request the Examiner withdraw the 35 U.S.C. §103(a) rejection of Claims 6 and 13 and allow issuance thereof.

III. Rejection of Claims 7 and 14 under 35 U.S.C. §103

The Examiner has rejected Claims 7 and 14 under 35 U.S.C. §103(a) as being unpatentable over Arnold in view of U.S. Patent No. 5,835,960 to Keene, *et al.* (Keene). As discussed above Arnold does not teach or suggest a multi-protocol bus system employing a plurality of protocol indicators associated with an address space, each of the plurality of protocol indicators associated with a segment of the address space and indicate a particular bus protocol of an external device as recited in independent Claims 1 and 8. Keene is directed to interfacing a ROM BIOS to a system bus having a data width greater than the memory width of the ROM BIOS. (Column 1, lines 9-11). Keene has not been cited to cure the deficiencies of Arnold but to teach dividing a PCI address space into 32 kilobyte address ranges. (Examiner's Action, page 4). Thus, the cited combination of

Arnold and Keene does not teach or suggest each and every element of independent Claims 1 and 8.

Since the cited combination of Arnold and Keene fails to teach or suggest each and every element of independent Claims 1 and 8 Claims dependent thereon, Claims 7 and 14 are not obvious in view of the cited combination. Accordingly, the Applicants respectfully request the Examiner withdraw the 35 U.S.C. §103(a) rejection of Claims 7 and 14 and allow issuance thereof.

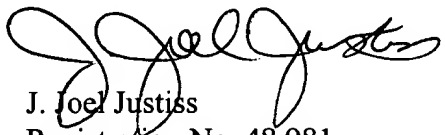
IV. Conclusion

In view of the foregoing amendment and remarks, the Applicants now believe that all of the Claims currently pending in this application are in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-21.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

HITT GAINES, P.C.



J. Joel Justiss
Registration No. 48,981

Dated: 6/30/04

P.O. Box 832570
Richardson, Texas 75083
(972) 480-8800